What is claimed is:

1. A system for providing coverage analysis of functional verification of integrated circuit designs comprising:

a) a test generator that creates test programs using machine readable test attribute specifications;

b) a simulator that compares the test programs against the simulated behavior of design models;

c) a database containing the traces of the simulation generated by the verification process;

d) a program for mining and analyzing the simulation database;

e) a database of all test programs generated by the test generators and engineers;

f) a program for mining and analyzing the test program database;

g) a database of all functional coverage analysis data and coverage model results;

h) a program for mining and analyzing the functional coverage database;

i) a program for analysis and monitoring of the coverage models;

j) a program for automatic test spec generation from design HDL;

k) a program for test spec adjustment and optimization;

l) a coverage analysis program for creating architectural coverage models of the test programs; and

m) functional coverage database for storage of the created coverage models.

2. The system according to claim 1 wherein the test programs are developed by the test generator based on specifications that are received from a test specification generator.

3. The system according to claim 2 wherein the test spec generator receives feedback from the simulation traces database mining, the test program database mining, and the coverage database mining modules.

4. The system according to claim 1 wherein the input to the simulator is based on the development of deterministic tests, and a program for mining and analyzing the simulation database includes the capability of providing feedback information for tuning these deterministic tests.

5. The system according to claim 1 wherein the coverage analysis serves to detect verification trends and patterns and to report the same.

6. The system according to claim 5 including a coverage report generator based on the information in the functional coverage database and the result of the analysis and mining of the said database wherein the actual verification process trends and patterns discovered are fedback to the test generator, to the coverage analysis environment, to the functional coverage database, and to the coverage report generator.

7. The system according to claim 1 further including a high level description of the design specification for the generation of machine readable coverage analysis models.

8. The system according to claim 7 further including a finite state machine and design state event extractor, and a coverage model generator using these as input to generate new coverage analysis models or update existing models.

9. A method for coverage analysis of functional verification of integrated circuit designs comprising the steps of

a) generating test programs using machine readable design specifications, and storing the test programs in a database;

b) comparing the test programs against the design models to produce simulation traces, and storing the resultant traces in a database;

c) mining and analyzing the test program database and the simulation traces database; and

d) creating architectural coverage models and microarchitectural coverage models, and storing the models in a functional coverage analysis environment.

10. The method according to claim 9 including the step of generating the test programs based on the optimized test specs.

11. The method according to claim 10 wherein the generation of the tests is also based on feedback from the analysis and mining of the test programs database, the simulation traces database, and the functional coverage database.

12. The method according to claim 9 further including the steps of developing deterministic tests, and providing feedback to these tests, based on the mining and analysis of the simulation traces database.

13. The method according to claim 9 further including the use of the analysis and mining of the functional coverage database to detect and report trends and patterns of interest to verification.

14. The method according to claim 13 wherein some of the architectural coverage models and microarchitectural coverage models are generated manually whereas other models are computer generated.

15. The method according to claim 9 wherein coverage reports are interpreted and made available to user via a plurality of interface devices and medium.

16. The method according to claim 15 wherein coverage directives are generated indicating tasks to be performed requiring certain skills and design knowledge.

17. The method according to claim 16 wherein generated reports, advisories, and directives are disseminated according to predefined methods and media protocols.

18. An article of manufacture comprising a computer usable medium having a computer readable program embodied in said medium, wherein the computer readable program, when executed on a computer, causes the computer to:

a) generate a test spec based upon predetermined design model, and forward the test spec to a test generator,

b) create a test program based on the test spec and store the test program in a test programs database;

c) forward each test program and manually generated tests to a simulator;

d) simulate the test program and tests against the design model, and generate a trace of the simulation;

e) store the traces in a simulation traces database;

f) mine the simulation traces for patterns;

g) mine data in the test programs database;

h) analyze data received from the test programs database, the simulation traces database and from the database mining, and generate new models if required, based on the presence or absence of a model; and

i) store the models in a functional coverage database.

19. The article of manufacture according to claim 18 wherein the computer readable program further causes the computer to generate design specs, and to generate coverage models based on these specs.

20. The article of manufacture according to claim 19 wherein the generated coverage models may be used based on the analysis of the test program database and the simulation traces database, and the mining of said databases.